22 Οκτωβρίου 2025

Λογική Σχεδίαση

Δυαδική λογική
Λογικές πύλες


Any
Questions

Σημαντική ημερομηνία

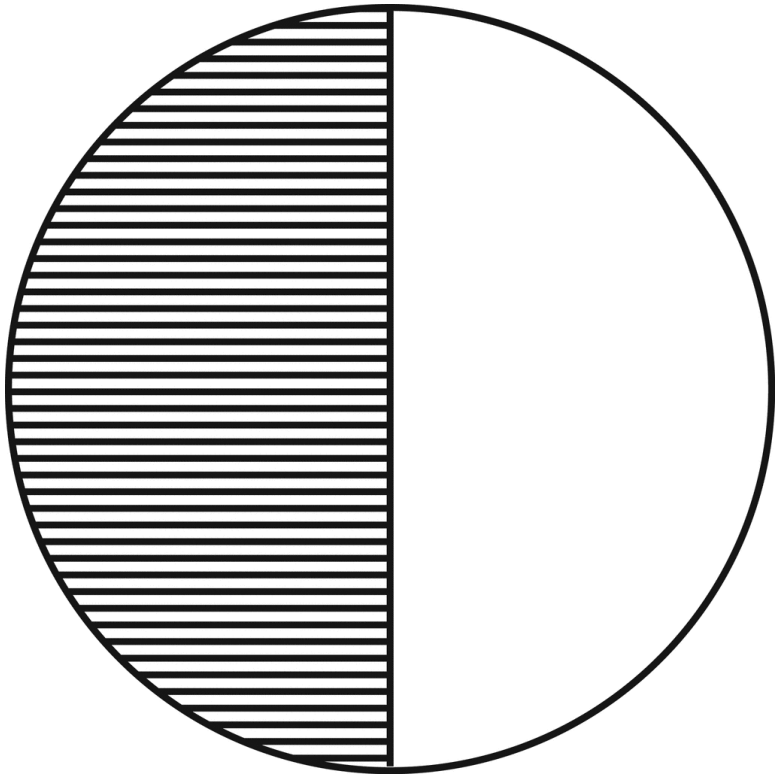
- **Τετάρτη, 29 Οκτωβρίου**
  - Απλοποίηση και ελαχιστοποίηση δυαδικών συναρτήσεων

yz / wx	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

Σημαντική ημερομηνία

- **Τετάρτη, 26 Νοεμβρίου, 09:00**
  - Εξέταση προόδου. Προσοχή στην ώρα!!

Δυαδική λογική



Bit

- bit – **bi**nary digi**t**
  - **1** / **0**

- Ναι / Όχι
- Σωστό / Λάθος
- Άσπρο / Μαύρο
- κλπ.

Μεταβλητές

- x
- HavingUmbrella
- CurrentlyRaining
- Tall
- Happy

Πράξεις

- OR
  - x + y
    - **δεν το διαβάζουμε «και»!**
- AND
  - x * y
  - xy
    - **επίσης δεν το διαβάζουμε «και»!**
- NOT ’
  - x'

Προτεραιότητα πράξεων

1. ()
2. ’
3. *
4. +

HavingUmbrella + CurrentlyRaining’

HavingUmbrella OR (NOT CurrentlyRaining)

Πίνακας αληθείας

AND

x	y	xy
0	0	0
0	1	0
1	0	0
1	1	1

OR

x	y	x+y
0	0	0
0	1	1
1	0	1
1	1	1

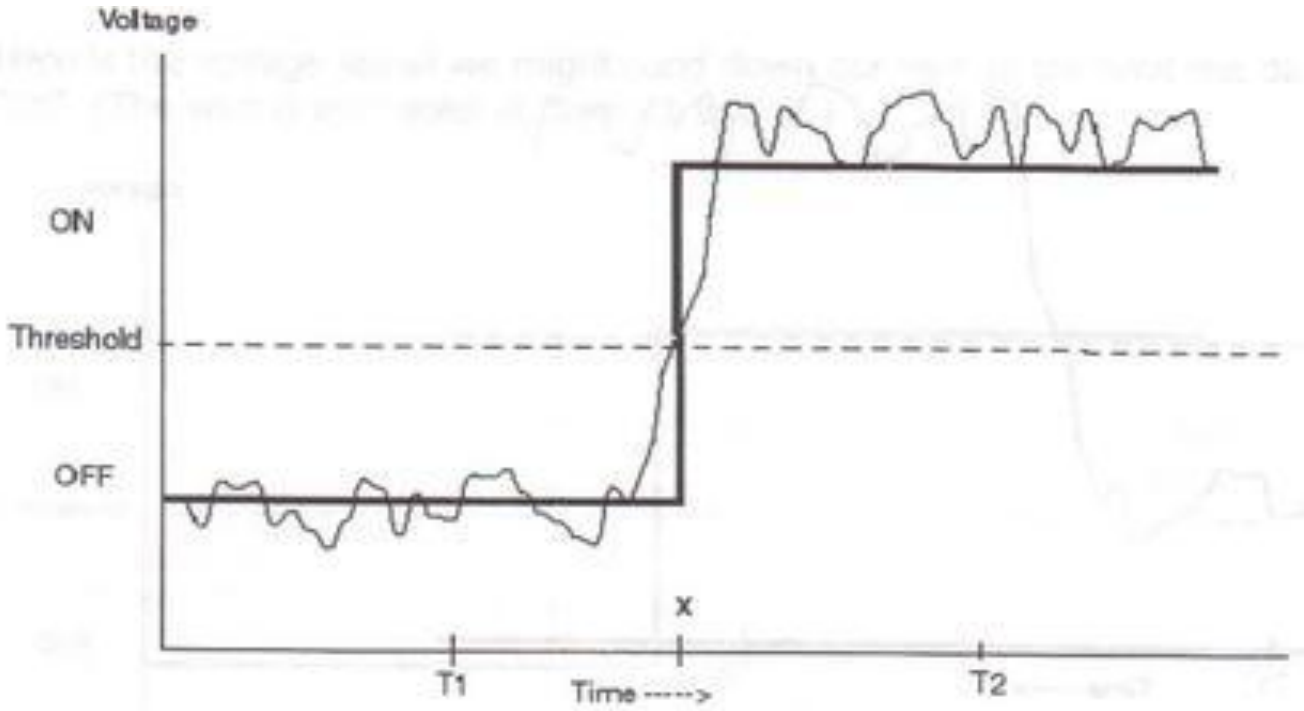
NOT

x	x’
0	1
1	0

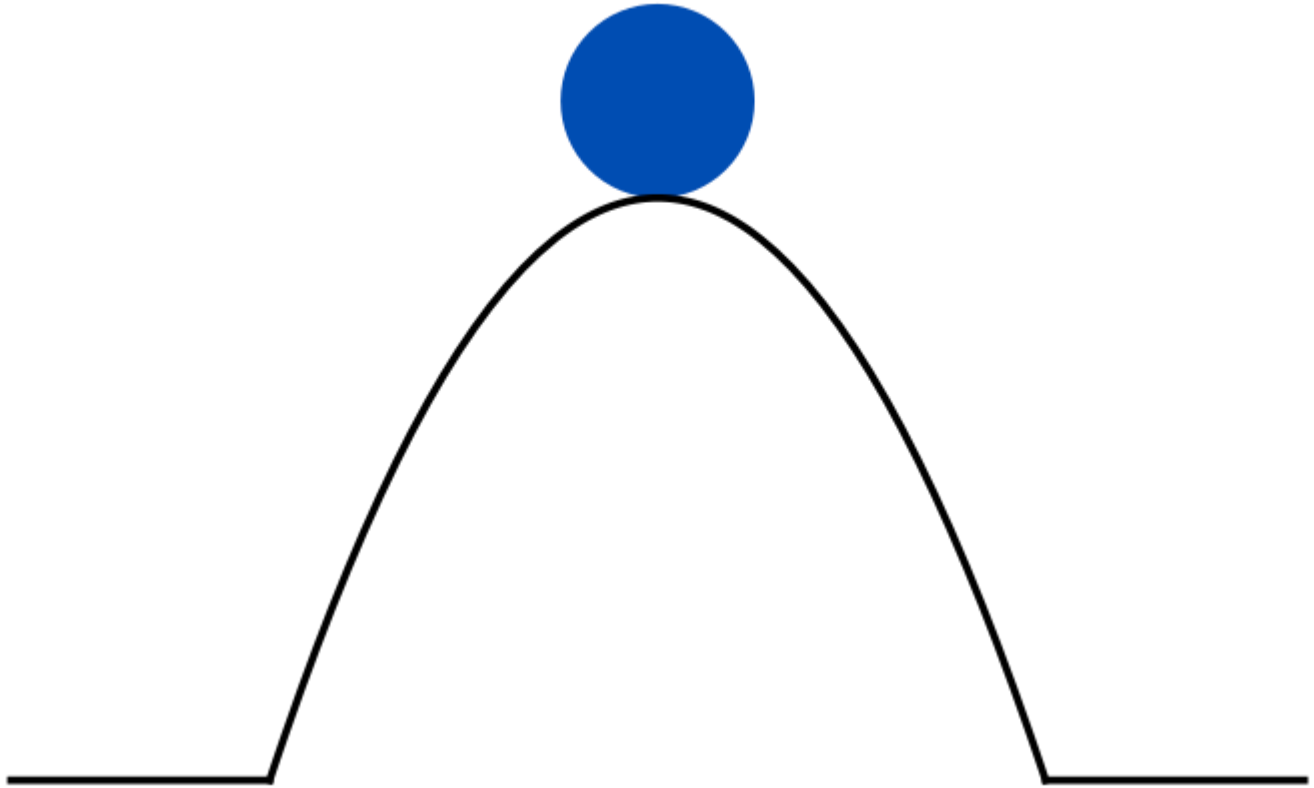
Λογικές πύλες

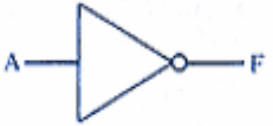
- Ηλεκτρονικά κυκλώματα

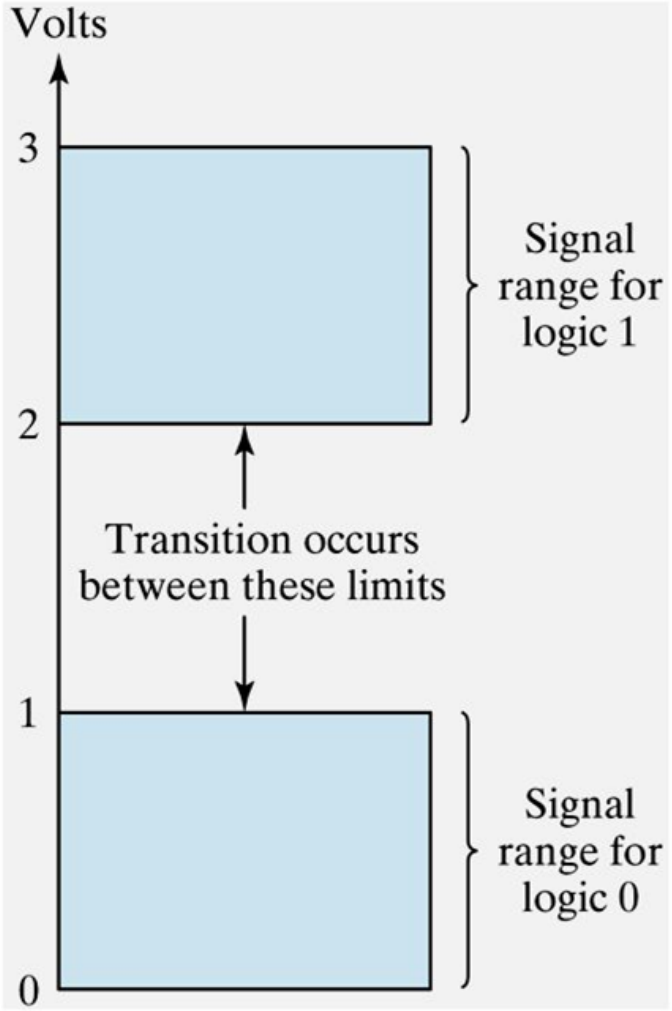
- Μία ή περισσότερες είσοδοι
- Μία έξοδος
- 2 διακριτές περιοχές τιμών



Noisy Signal

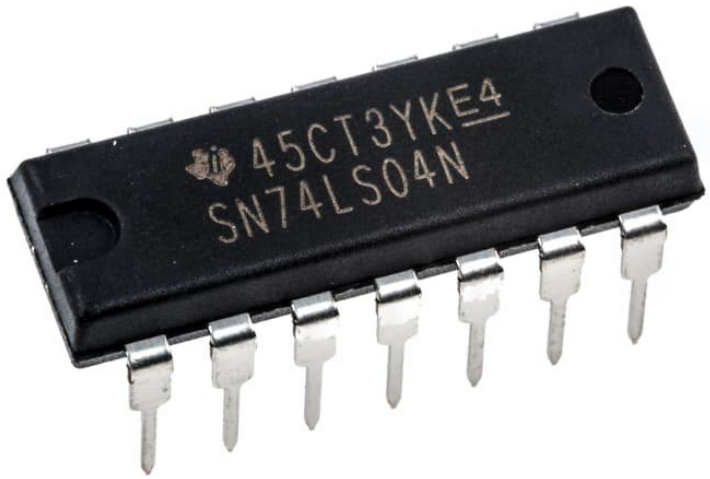


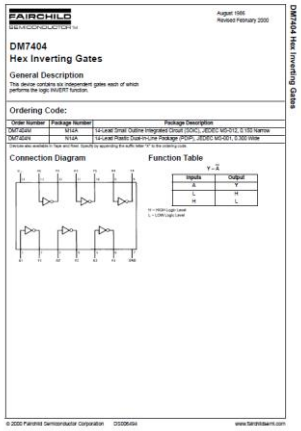
Name	Graphic Symbol	Algebraic Function	Truth Table
AND		$F = A \cdot B$ or $F = AB$	A B | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1
OR		$F = A + B$	A B | F 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1
NOT		$F = \overline{A}$ or $F = A'$	A | F 0 | 1 1 | 0
NAND		$F = (\overline{AB})$	A B | F 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
NOR		$F = (\overline{A + B})$	A B | F 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0


Volts
3
2
1
0
Signal range for logic 1
Transition occurs between these limits
Signal range for logic 0

IRL

- Πύλη NOT





FAIRCHILD SEMICONDUCTOR™

August 1986
Revised February 2000

DM7404 Hex Inverting Gates

DM7404
Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM7404M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM7404N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

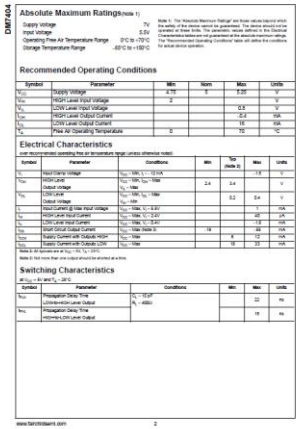
Function Table

$Y = \overline{A}$

Inputs	Output
A	Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

© 2000 Fairchild Semiconductor Corporation DS006464 www.fairchildsemi.com



DM7404

Absolute Maximum Ratings(Note 1)

Supply Voltage 7V
Input Voltage 5.5V
Operating Free Air Temperature Range 0°C to +70°C
Storage Temperature Range −65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Norm	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = MAX, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = MAX, V_I = 2.4V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = MAX, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = MAX (Note 3)	−18		−55	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = MAX		6	12	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = MAX		18	33	mA

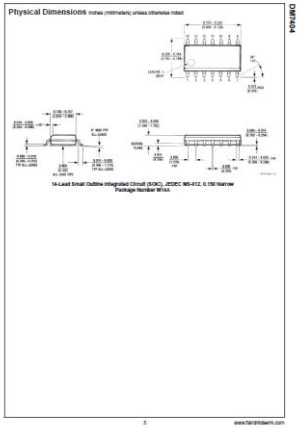
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF, R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			15	ns

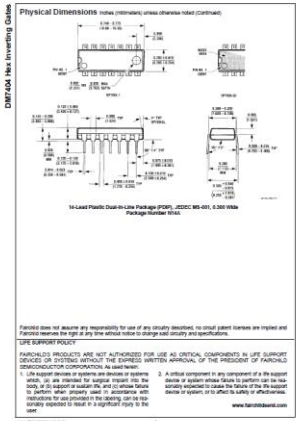


DM7404

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M14A

3 www.fairchildsemi.com



DM7404 Hex Inverting Gates

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

4

FAIRCHILD
SEMICONDUCTOR

August 1986
Revised February 2000

DM7404
Hex Inverting Gates

DM7404 Hex Inverting Gates

General Description

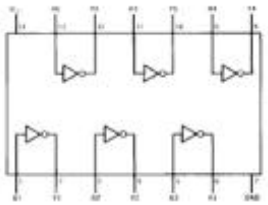
This device contains six independent gates each of which performs the logic INVERT function.

Ordering Code:

Order Number	Package Number	Package Description
DM7404M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM7404N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

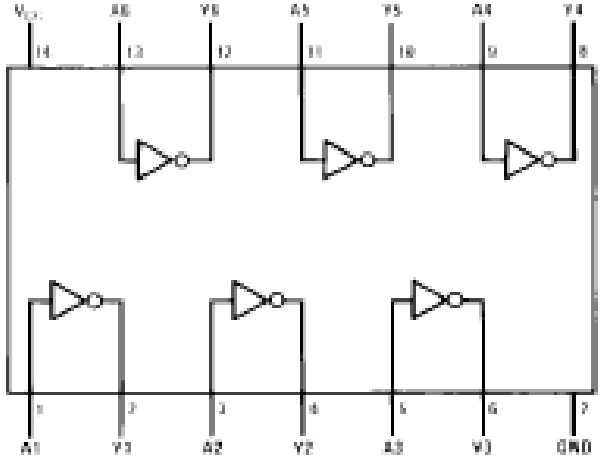
$Y = \overline{A}$

Inputs A	Output Y
L	H
H	L

H = HIGH Logic Level
L = LOW Logic Level

 DS006494 www.fairchildsemi.com

Connection Diagram



Function Table

$Y = \overline{A}$

Inputs A	Output Y
L	H
H	L

DM7404

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-0.4	mA
I_{OL}	LOW Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = -12 mA			-1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			-1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	-18		-55	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		6	12	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		10	23	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

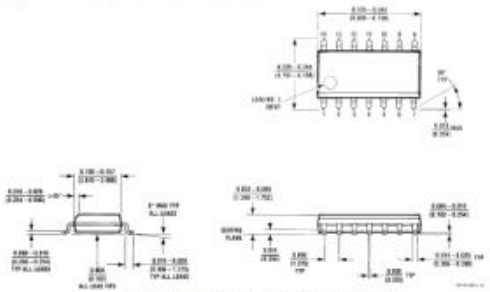
Note 3: Not more than one output should be shorted at a time.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

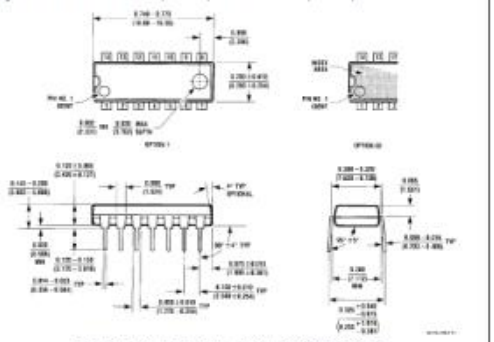
Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF, R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			15	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

Άλλες πύλες

- Δυνατότητα και κόστος
- Μαθηματικές ιδιότητες
  - Δυνατότητα επέκτασης αριθμού εισόδων
  - Χρηστικότητα

Θέματα υλοποίησης

- Θετική και αρνητική λογική
- Επίπεδα ολοκήρωσης
  - Small Scale Integration (SSI)
    - <10
  - Large Scale Integration (LSI)
    - <10.000
  - Very Large Scale Integration (VLSI)
    - >10.000

Οικογένειες

- Transistor-Transistor Logic (TTL)
  - Πρότυπη
- Emitter-Coupled Logic (ECL)
  - Ταχύτητα
- Metal-Oxide-Semiconductor (MOS)
  - Πυκνότητα
- Complementary MOS (CMOS)
  - Κατανάλωση

Μέτρα απόδοσης

- Fan-in
- Standard load
- Fan-out
- Power dissipation
- Propagation delay
- Noise margin