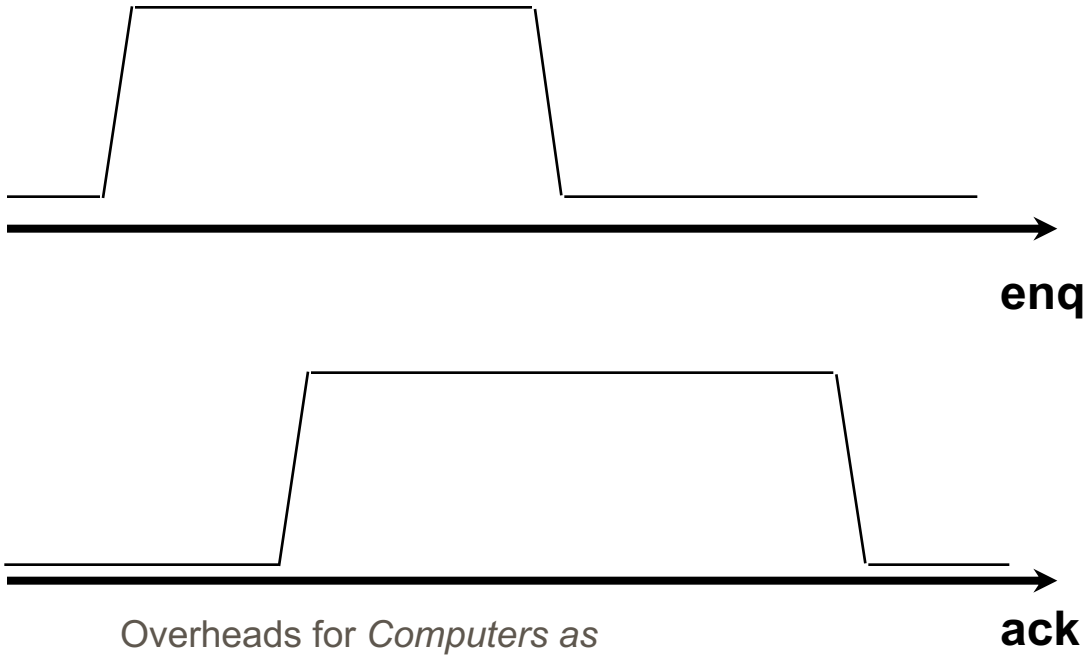
System components

- Timing diagrams.
- Memory.
- Busses and interconnect.

Timing diagrams

- A timing diagram shows a trace through the operation of a system.
  - Generally used for asynchronous machines with timing constraints.

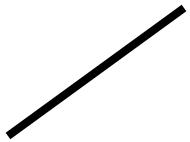


Timing diagram syntax

- Constant value:

- Stable:

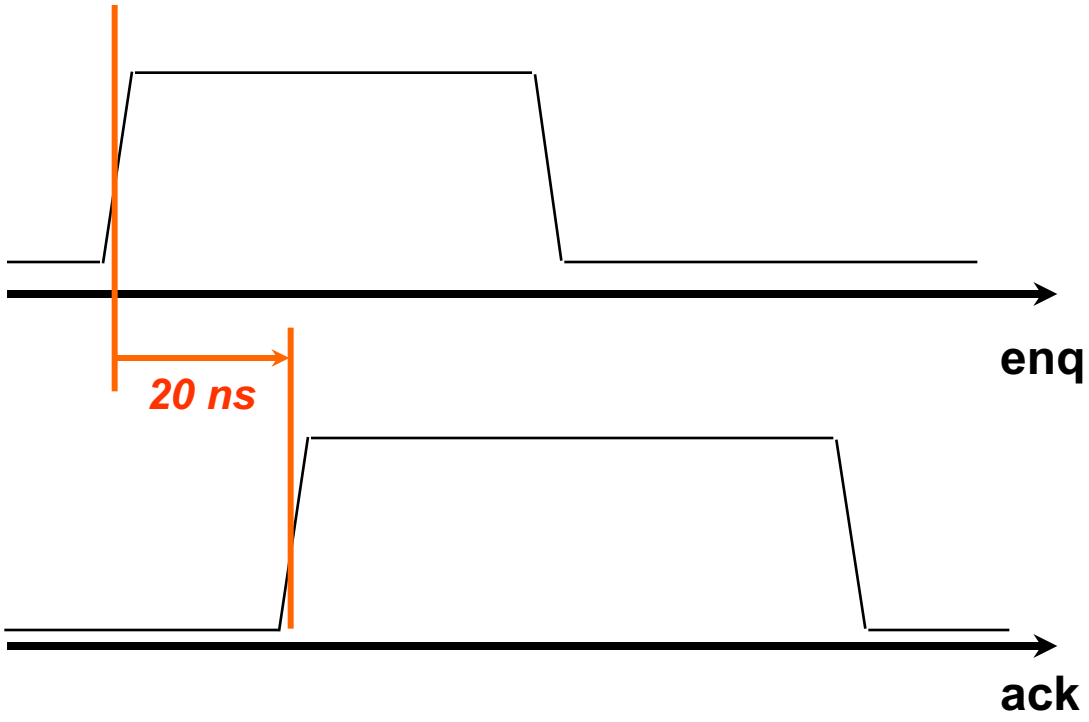
- Changing:



- Unknown:

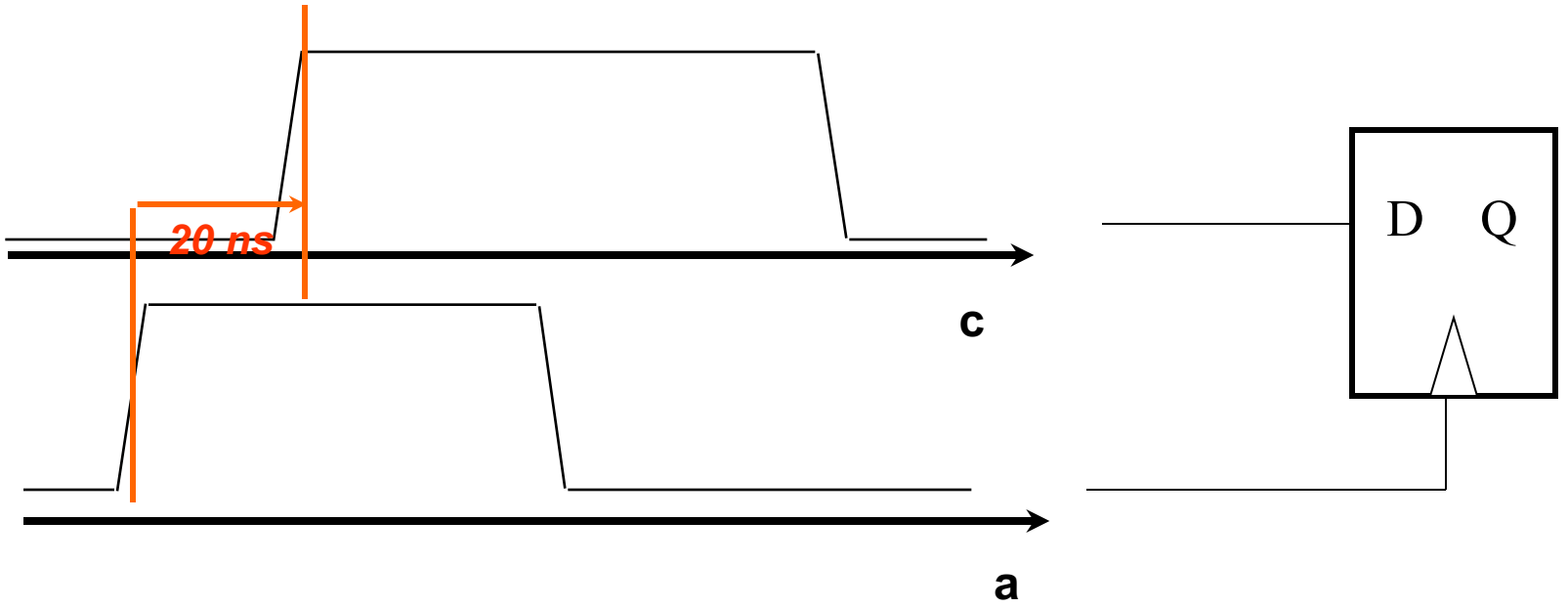
Timing constraints

- Minimum time between two events:

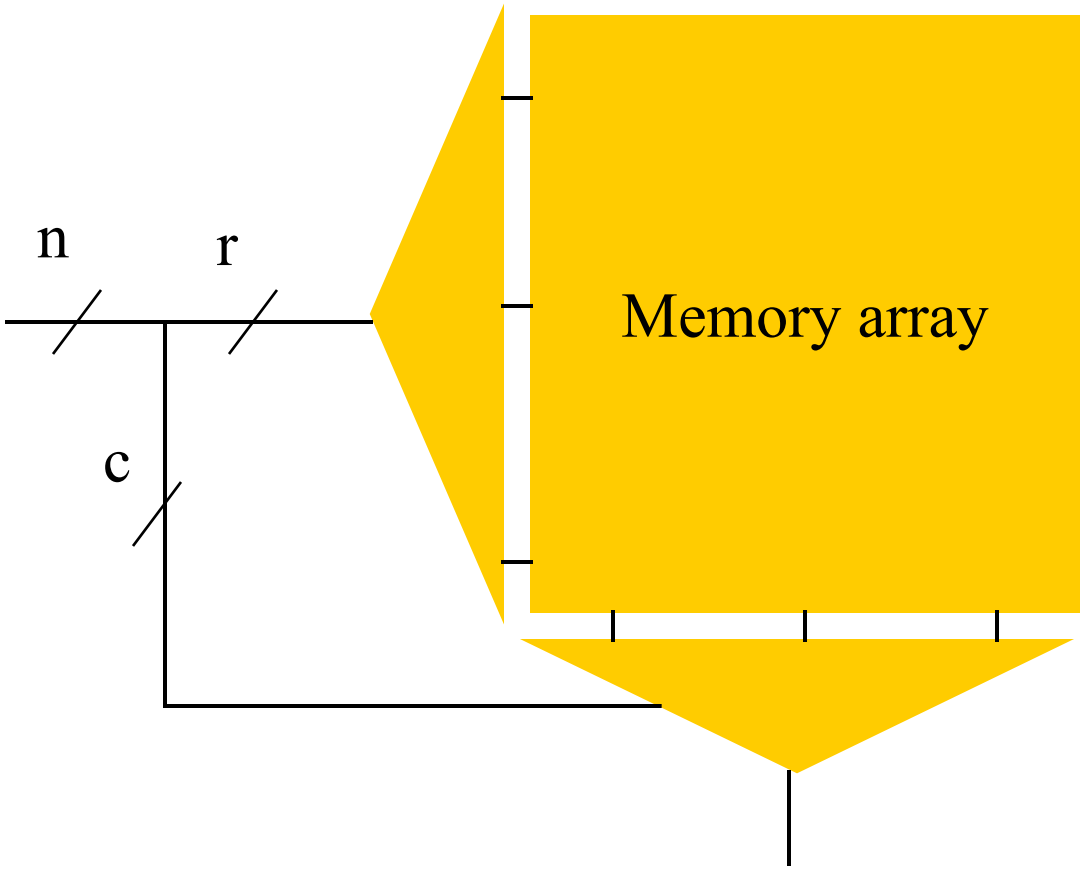


Origin of timing constraints

- Control signals are passed on the bus:



Memory device organization



Memory parameters

- Size.
  - Address width.
- Aspect ratio.
  - Data width.

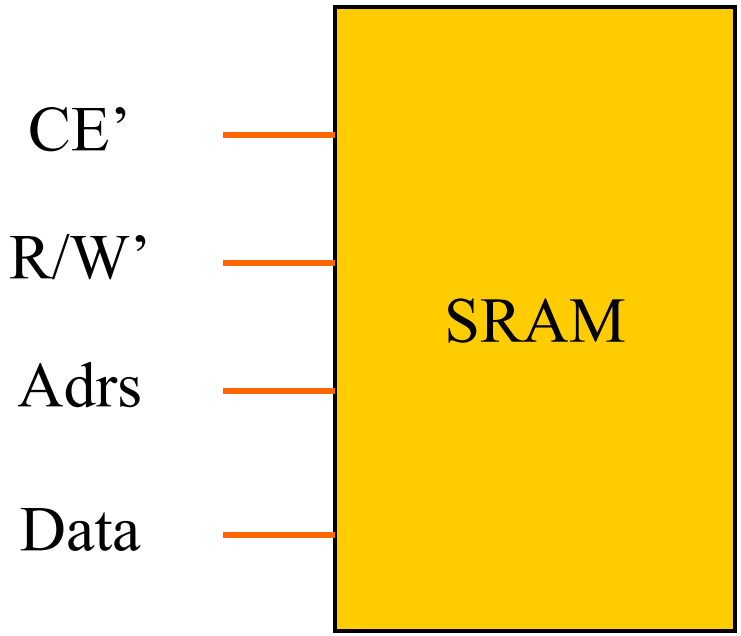
Types of memory

- ROM:
  - Mask-programmable.
  - Flash programmable.
- RAM:
  - DRAM.
  - SRAM.

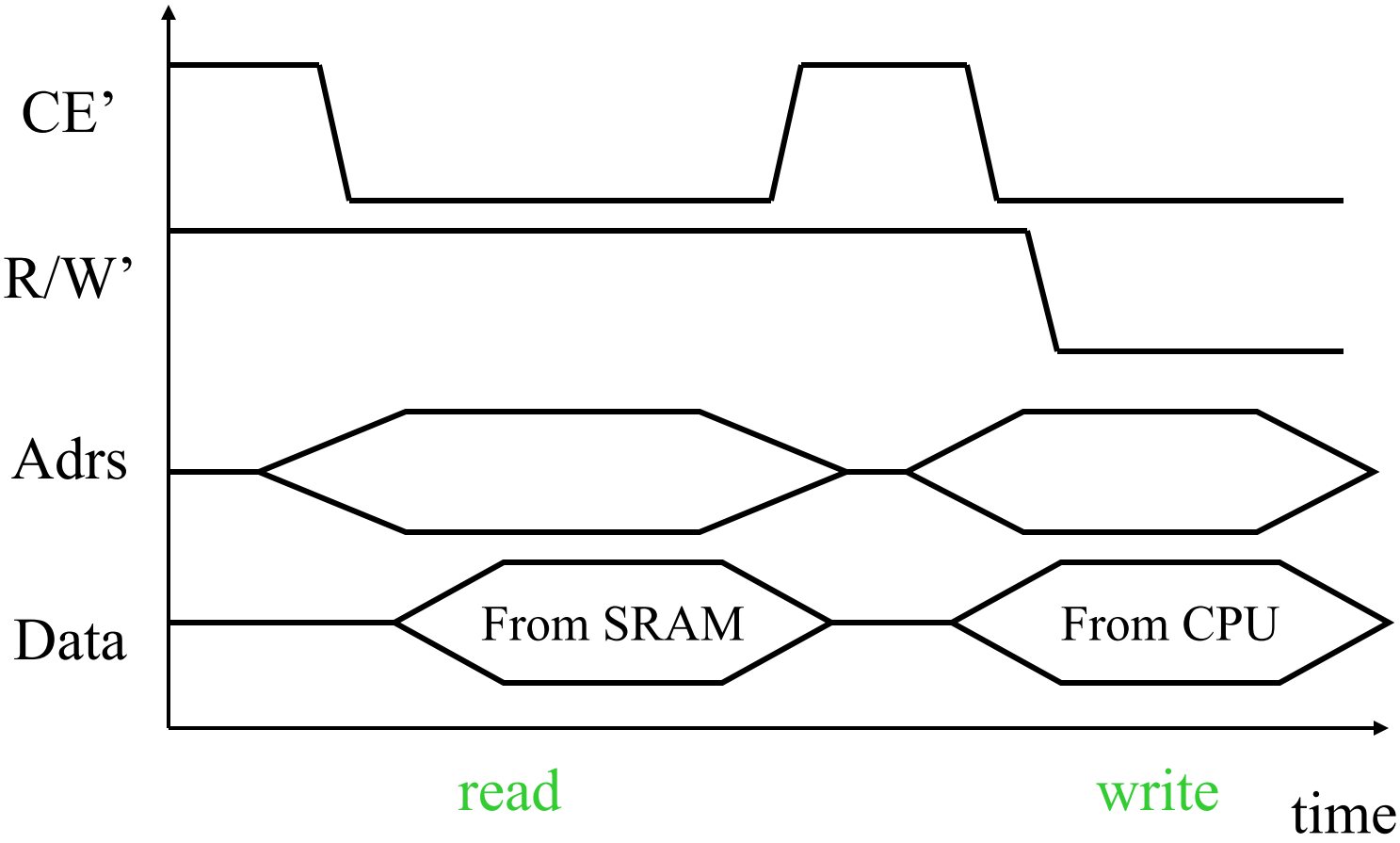
SRAM vs. DRAM

- SRAM:
  - Faster.
  - Easier to integrate with logic.
  - Higher power consumption.
- DRAM:
  - Denser.
  - Must be refreshed.

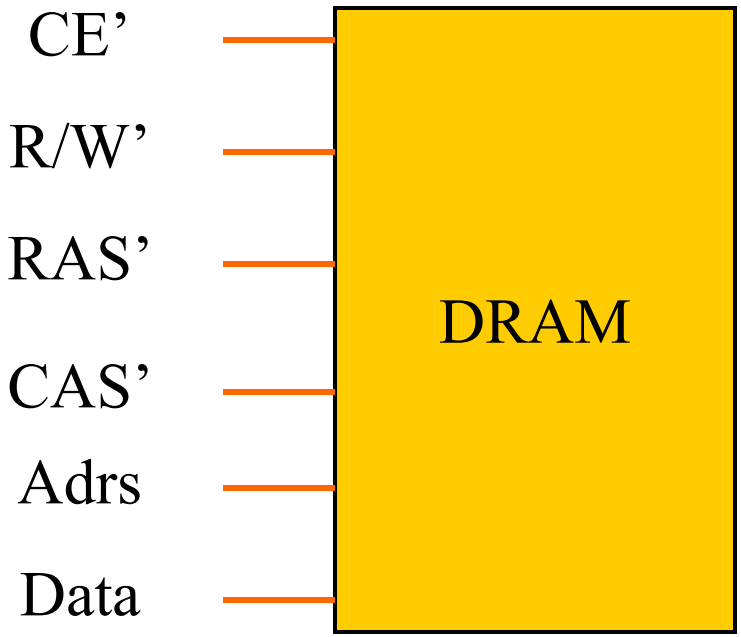
Typical generic SRAM



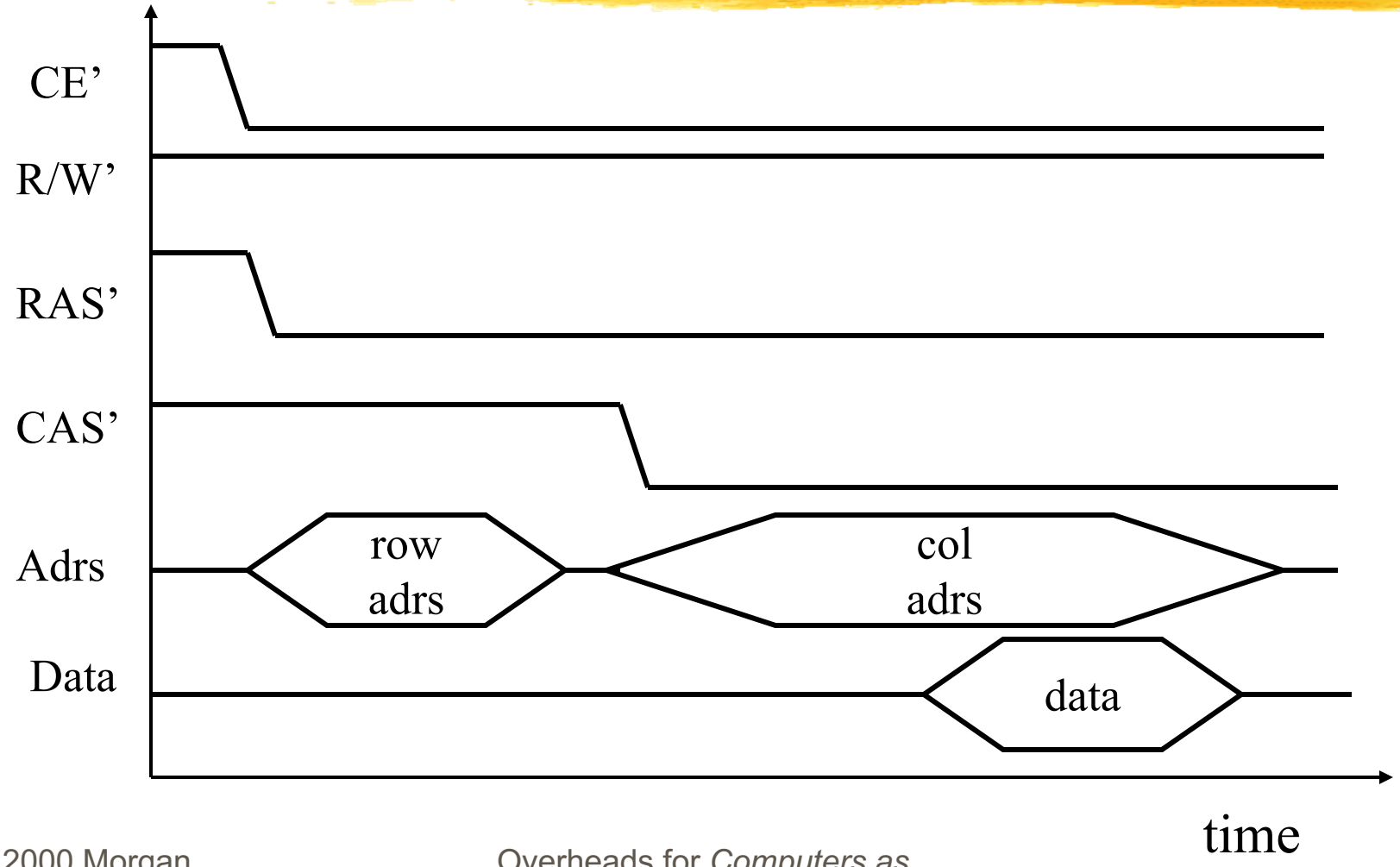
Generic SRAM timing



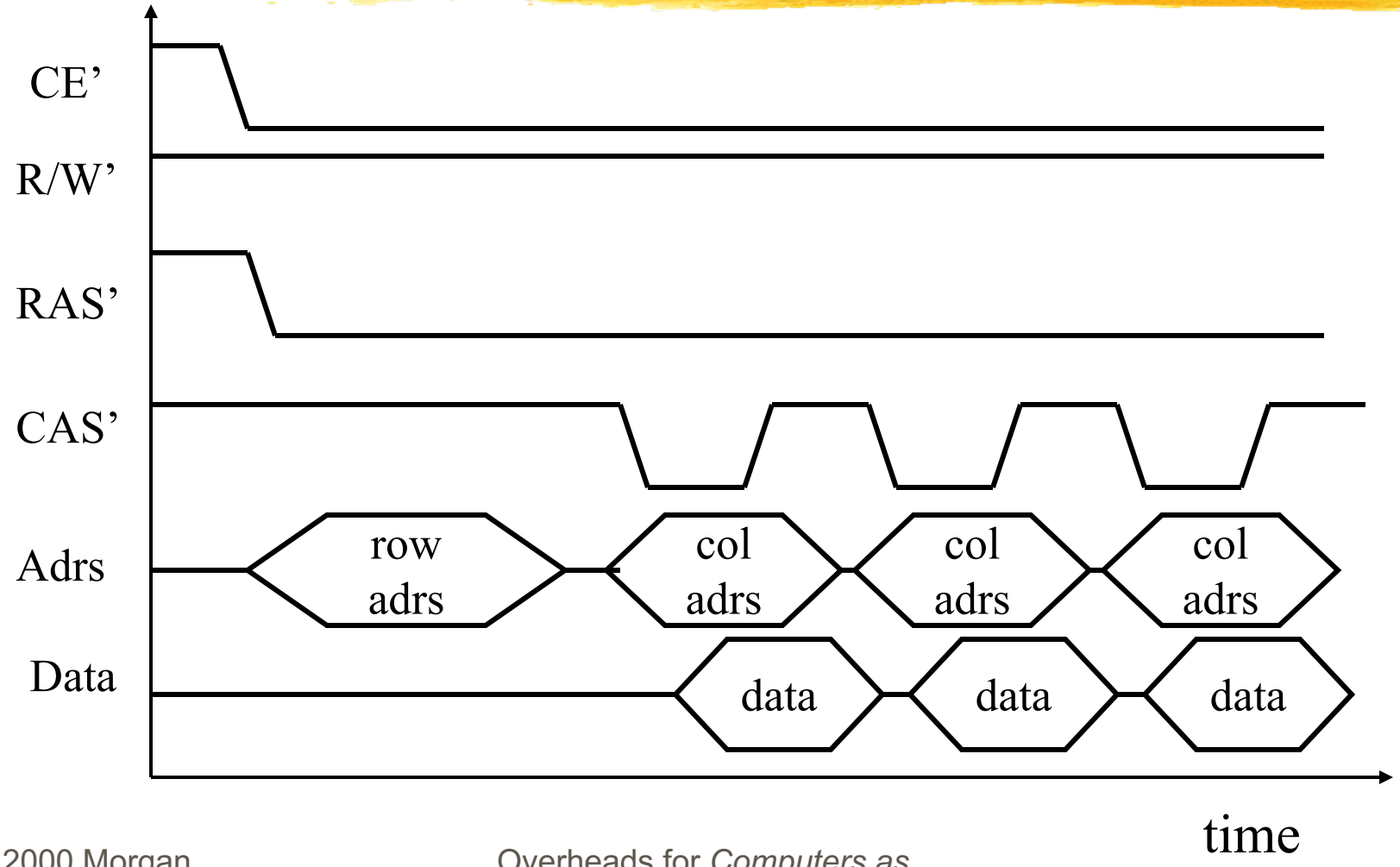
Generic DRAM device



Generic DRAM timing



Page mode access



RAM refresh

- Value decays in approx. 1 ms.
- Refresh value by reading it.
  - Can’t access memory during refresh.
- CAS-before-RAS refresh.
- Hidden refresh.

Other types of memory

- Extended data out (EDO): improved page mode access.
- Synchronous DRAM: clocked access for pipelining.
- Rambus: highly pipelined DRAM.

Flash issues

- Flash is programmed at system voltages.
- Erasure time is long.
- Must be erased in blocks.

Generic bus structure

- Address:

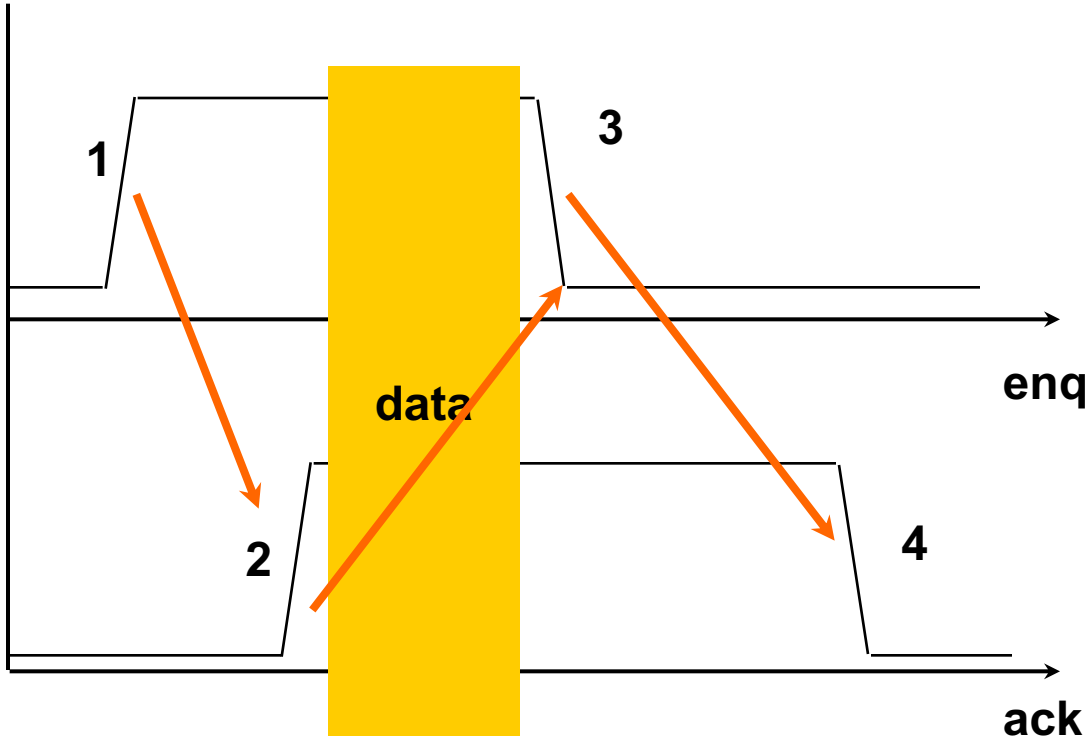
- Data:

- Control:

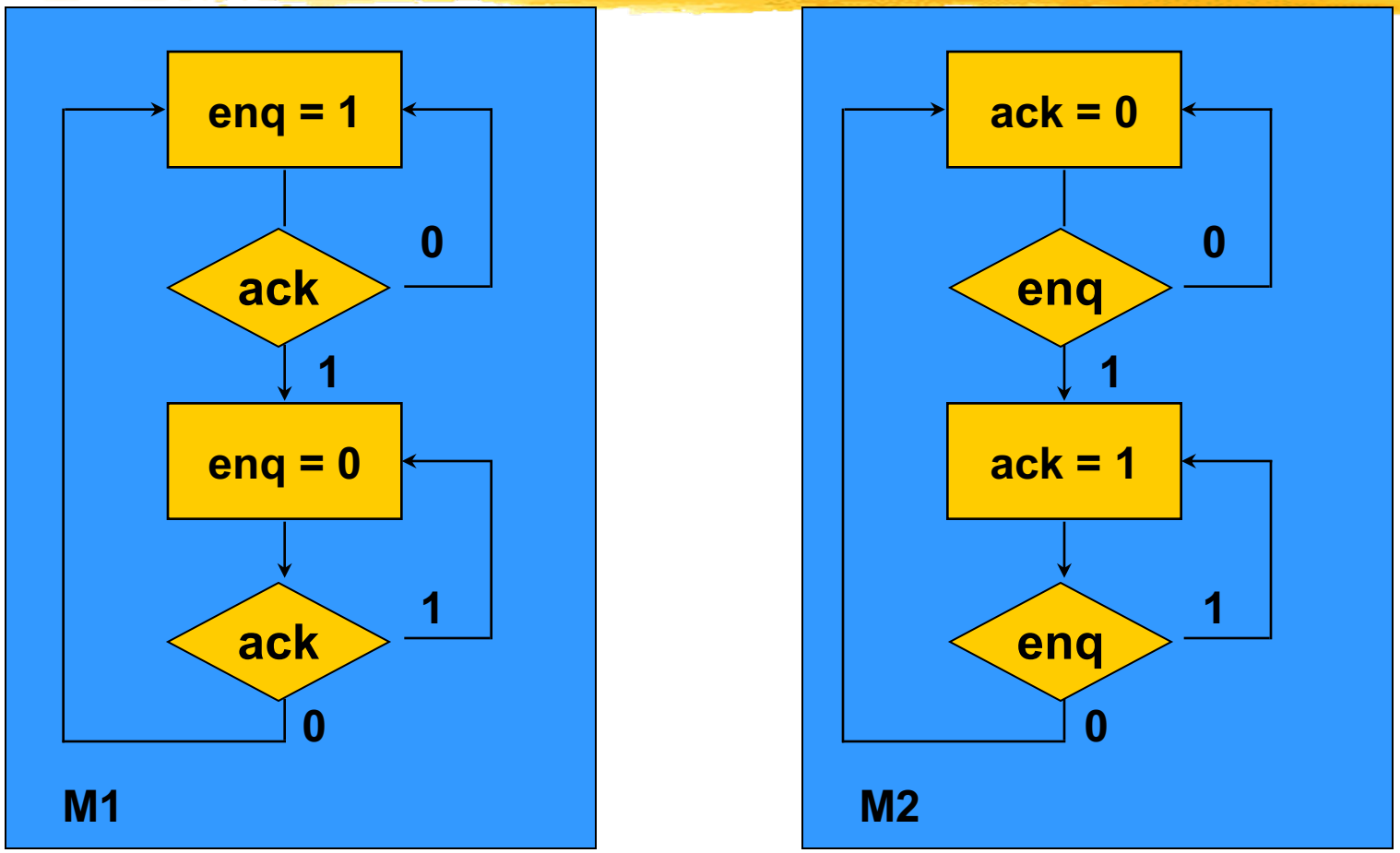
Electrical bus design

- Bus signals are usually tri-stated.
- Address and data lines may be multiplexed.
- Every device on the bus must be able to drive the maximum bus load:
  - Bus wires.
  - Other bus devices.
- Bus may include clock signal.
  - Timing is relative to clock.

Four-cycle handshake



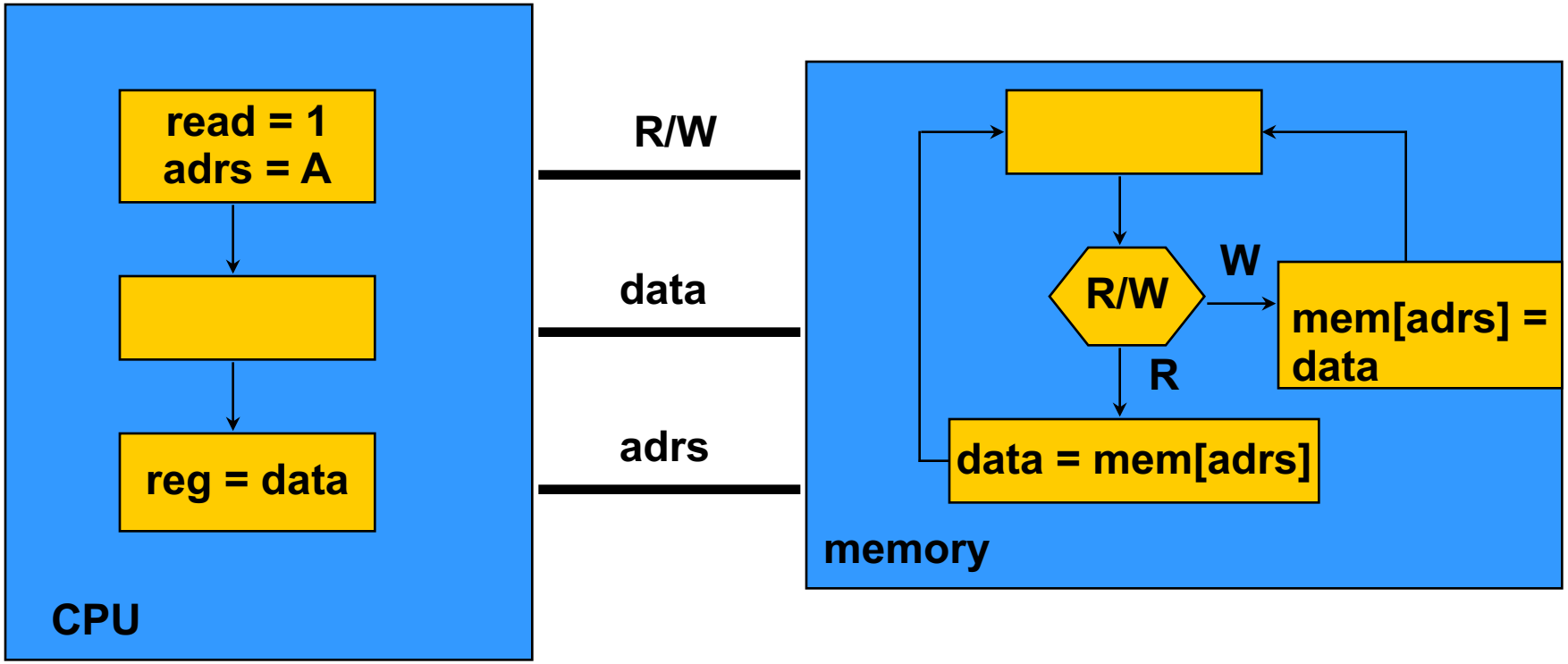
Busses as communicating machines



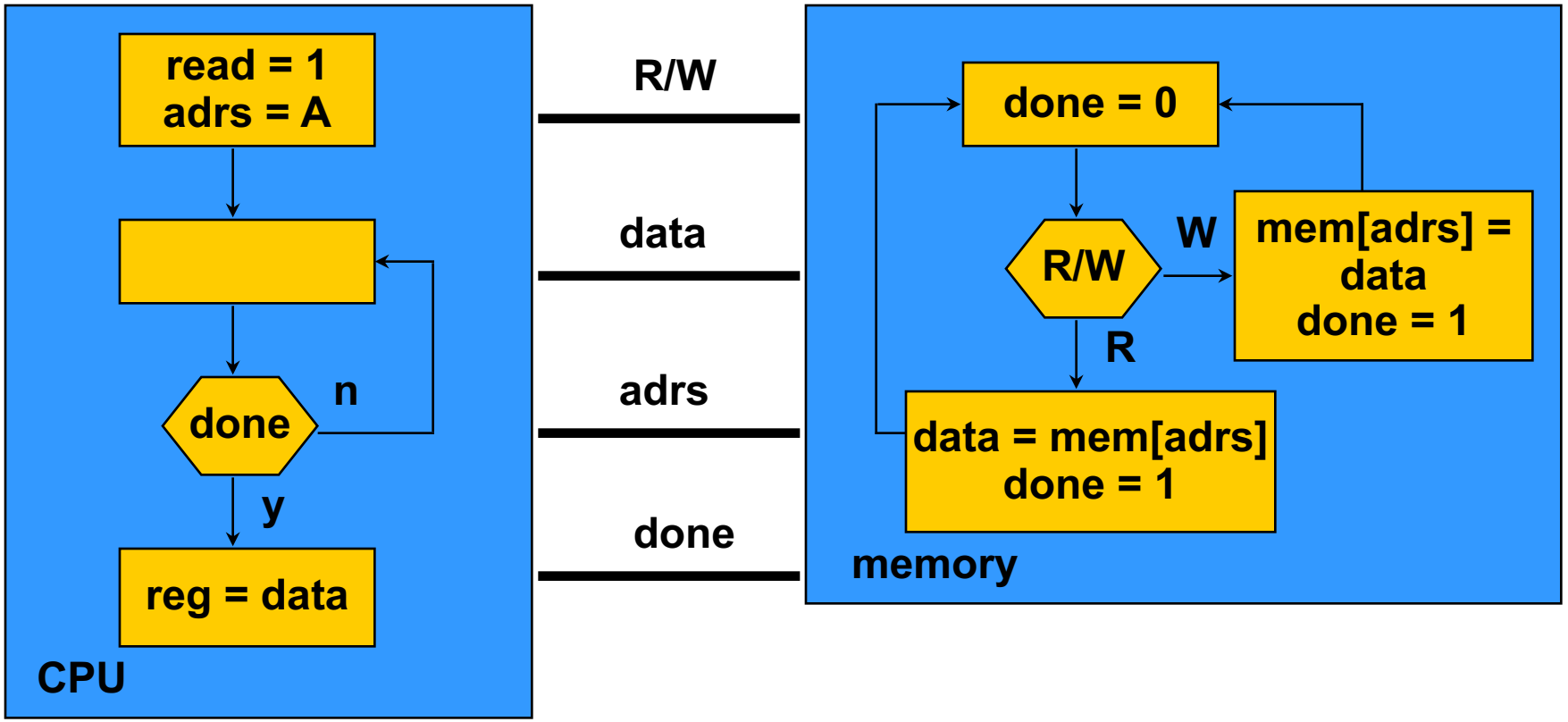
When should you handshake?

- When response time cannot be guaranteed in advance:
  - Data-dependent delay.
  - Component variations.

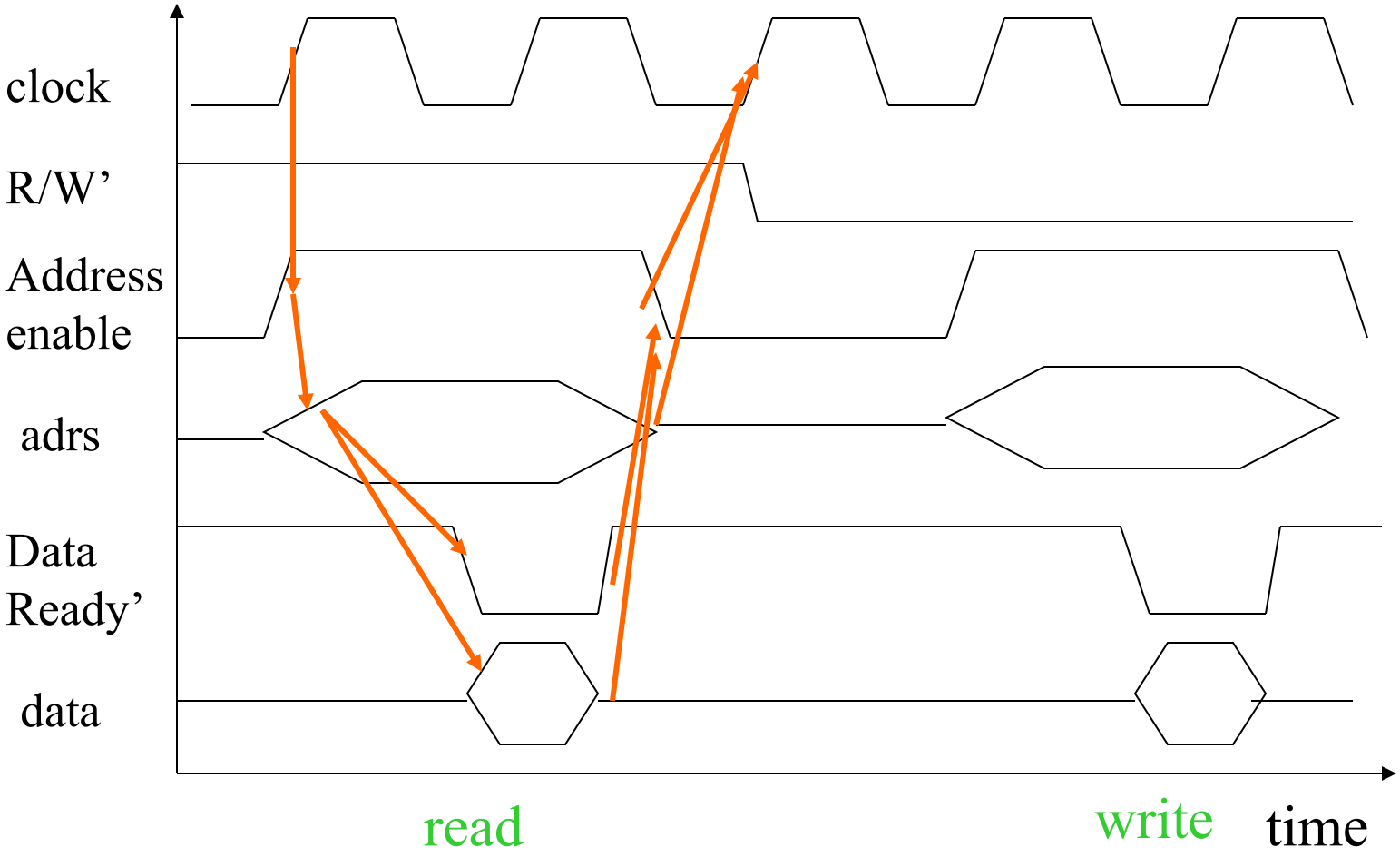
Fixed-delay memory access



Variable-delay memory access



Typical bus access

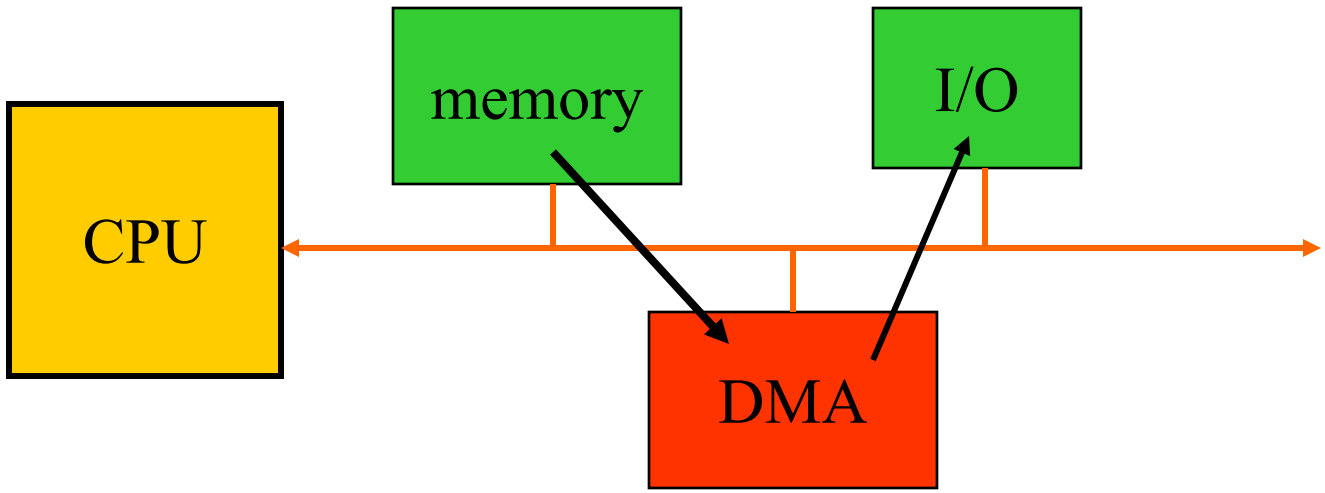


Bus mastership

- Bus master controls operations on the bus.
- CPU is default bus master.
- Other devices may request bus mastership.
  - Separate set of handshaking lines.
  - CPU can’t use bus when it is not master.

Direct memory access (DMA)

- DMA provides parallelism on bus by controlling transfers without CPU.



DMA operation

- CPU sets up DMA transfer:
  - Start address.
  - Length.
  - Transfer block length.
  - Style of transfer.
- DMA controller performs transfer, signals when done:
  - Cycle-stealing.
  - Priority.

ARM busses

- AMBA:
  - Open standard.
  - Many external devices.
- Two varieties:
  - AMBA High-Performance Bus (AHB).
  - AMBA Peripherals Bus (APB).