



Open Virtual Platforms (OVP) An Introduction and Overview

info@ovpworld.org

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The growing challenge

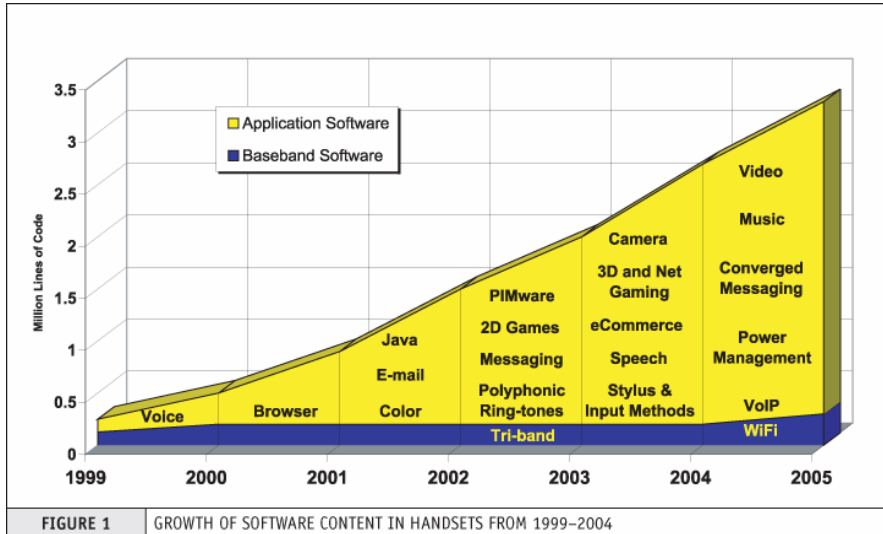


FIGURE 1 GROWTH OF SOFTWARE CONTENT IN HANDSETS FROM 1999-2004

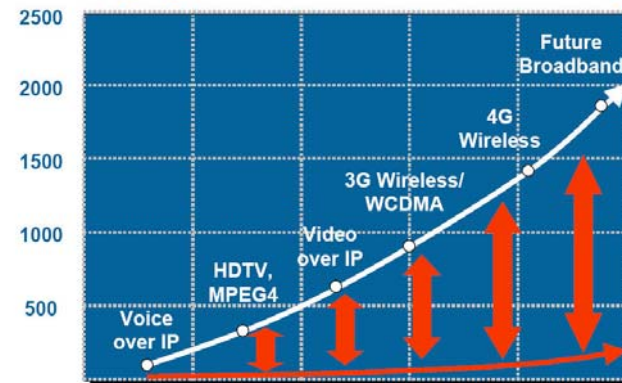
Examining the economics of building next-generation mobile handsets with Linux
By: Bill Weinber, Jun. 14, 2005 11:00 AM, linux.sys-con.com

- SW content of electronic products grows dramatically
 - Millions and millions lines code
 - In 2007 SW dev costs exceeds HW design costs for SoC ICs

- and the software needs to run faster and faster to provide more and more functionality

DSP Operations per second (Billion MAC/s)

Emerging Communications Technologies



DSP performance requirements for new communication technologies

Standard DSP Processor Performance Roadmap

Source: Xilinx

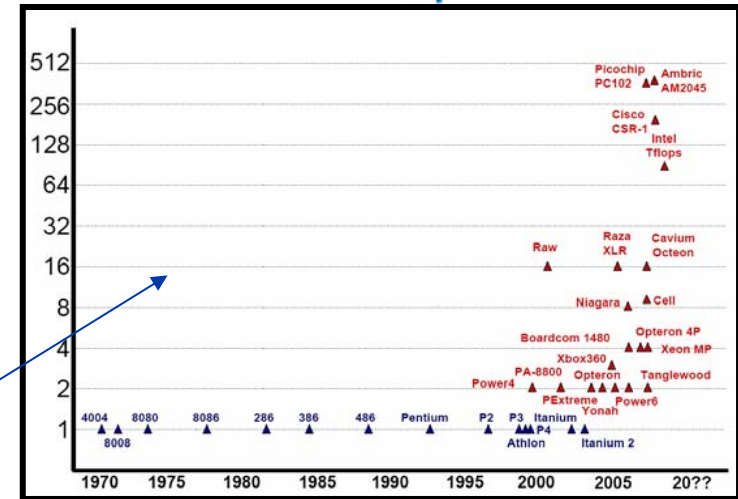
The real solution is Multi-Core



“Von Neumann is a poor use of scaling – all the energy is going on the communication between the processor and the memory. Its much better to use 20 microprocessors running at 100MHz than one at 2GHz”

Hugo de Man, IMEC

- Early movers have been building multi-core standard processors
- And more and more System on Chips (SoCs) and Platform chips are becoming multicore



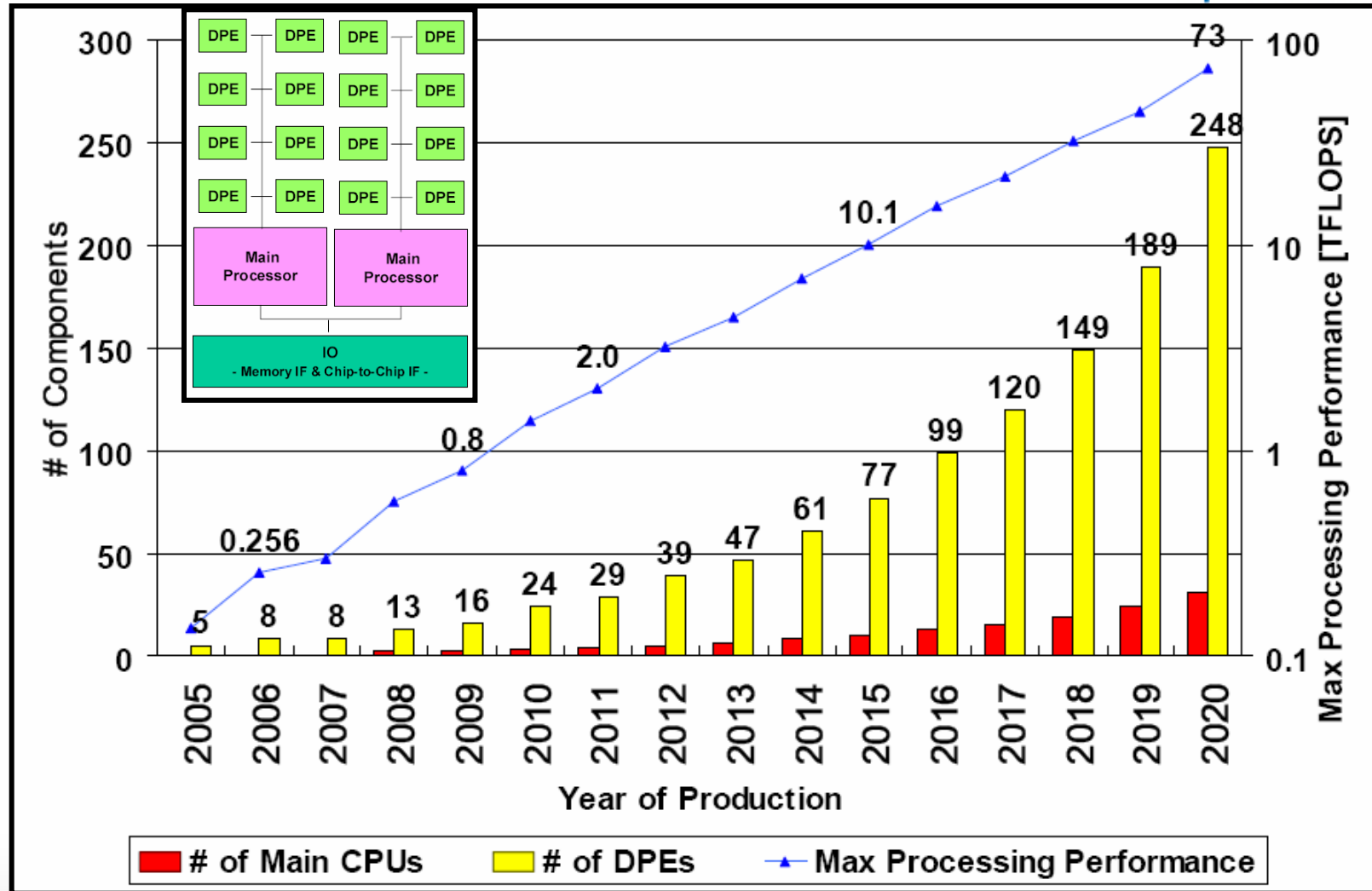
Key Trends

- ASIC/ASSP ratio: 80/20 in 2000, 50/50 now
 - In-house ASIC design is down
 - Replaced by off-the-shelf, programmable ASSP
- Number embedded processors in SoC rising:
 - ST: recordable DVD 5
 - Hughes: set-top box 7
 - Agere: Wireless base station 8
 - ST: HDTV platform 8
 - Latest mobile handsets 10
 - NEC: Image processor 128
 - In-house NPU >150



Philippe Magarshack, Pierre Paulin, Central R&D, STMicroelectronics

Processor count predicted to increase dramatically



Source: ITRS 2006 Update
DPE: Data Processing Engine

Embedded Software for MPSoCs: An extreme challenge!



“30 to 50 per cent of R&D budgets are spent on software, and the cost is rising 20 per cent a year. The software effort overtakes the hardware effort at 130nm.”

Jack Browne, MIPS Technologies

“Some say we are at a crisis stage with the software side overwhelming the hardware side. Driving some of this is the proliferation of cores in system-on-chip (SoC) devices.”

Steve Roddy, Tensilica

SW problems delay SoC revenues, impacting IP developer royalties

Productizing MPSoCs



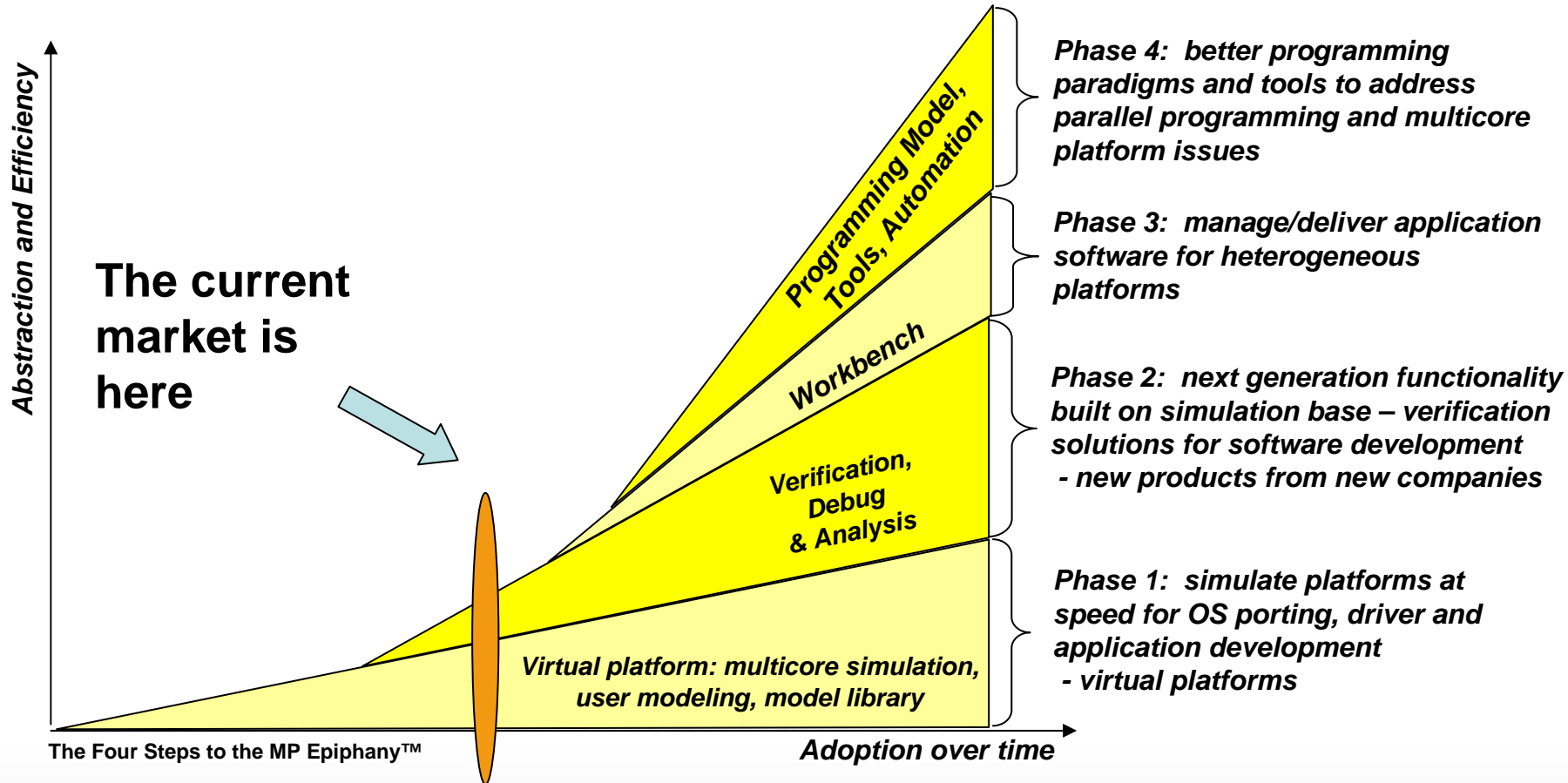
- So what does the future hold for software that is to run on these multi-core chips?
- Understanding what the future could look like, how can we make that better?

Current SoC (Software on Chip!) development methodology



- Start developing application software in parallel with hardware
 - But cannot test software
 - Get chip or FPGA on prototype board
 - The hardware is always far too late in the product development cycle
 - Also it is a limited, unreliable and not up to date prototype / platform
 - Connect up debugger to jtag port
 - Then there is a real challenge in verifying and debugging MP software
 - Lack of controllability, visibility, precision
 - And poor MP support
 - More and more teams scrabbling about in looking for a better solution
-
- ⇒ Moving to Virtual Platforms for earlier testing of software
 - ⇒ If initial testing of software is done on Virtual Platform, could reduce SoC schedule by months, and reduce initial development and maintenance costs significantly for SoC embedded software

Observation: New Embedded Software Development Tools needed (especially for multicore)



Virtual Platforms Market Grows Fast



- “Virtual Platform and simulation tools are the fastest growing segment of the electronic system level tools market ...”
 - “28 percent of respondents are using virtual prototyping today, and 44 percent expect to use it within the next two years.”
 - “The challenge of designing and testing software earlier in the design process is becoming an increasingly significant factor, especially in cases where the hardware environment may be extremely complex or not yet available.”
 - Matt Volckmann, Senior Analyst with VDC's embedded software practice,
- ⇒ Big demand currently and near future
- ⇒ But for what virtual platform technology?

Virtual Platforms Types



- Hardware Virtual Platforms
 - Timing / Cycle accurate
 - Used for architecture performance analysis, drivers, firmware
 - Models are very complex, slow, time consuming to build
 - SystemC etc
 - Main value is same performance as RTL, no Verilog license cost...

- Software Virtual Platforms
 - Instruction accurate
 - Used for OS, applications
 - Can be very fast, programmers views
 - Model only what is needed in peripherals
 - Complete system environment

What is needed?



- **Open way of modeling needed for Virtual Platforms**
 - Targeted at Instruction Accurate Software Virtual Platform need
 - Easy to use, high level, 100s of MIPS
 - Covers complexity of current designs easily
 - Built-in interoperability for models from different developers
 - Proven and in use technology
- **Methodology that leads to an ecosystem**
 - Ability to enable model builders to protect IP
 - Interfaces that enable the growth of tool chains
 - Tools that provide verification, debug, analysis of embedded sw
- **Backwards compatible with legacy solutions**

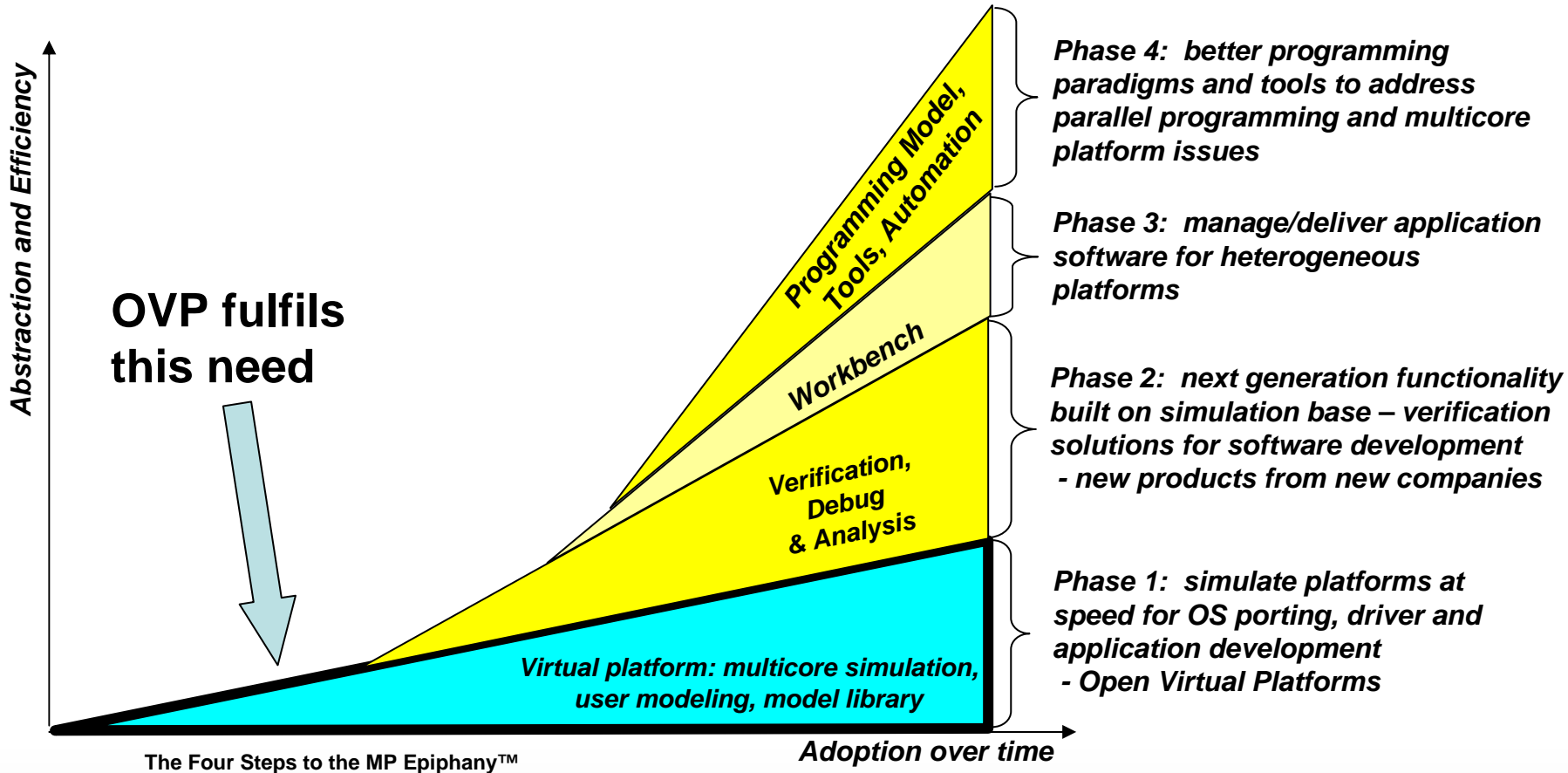
Introducing OPEN VIRTUAL PLATFORMS



- “Imperas believes that software virtual platform infrastructure should be open and be freely available.
- To that end, we are sharing, making public, and making open our simulation infrastructure technologies with the intention of establishing a common, open standard platform for software virtual platforms for software developers.
- We are also placing many complex processor and peripheral models in open source.
- Imperas will support and manage the OVP site, and will contribute much of our innovation to keep this infrastructure evolving.
- However, it is not solely through our efforts that these technologies become successful. Participation of organizations and individuals around the world is critical to the success of OVP.
- We offer our thanks to all those that are participating in this community.”

Simon Davidmann, CEO Imperas and OVP Founder

Virtual Platforms (OVP) are the foundation for the next generation of [embedded] software development environments – especially for multicore



Requirements on OVP Software Virtual Platforms



- Easy to create virtual platforms of MANY peripherals and MANY processors
- Easy to create your own processors, peripherals, platforms
- Library of processor and peripheral models
- Full programmers views, registers, addressing, interrupts
- Model only what is needed in peripherals
- Simulations are Instruction Accurate, very fast
- Used for application, OS, embedded software development
- Connect to 3rd party debuggers, e.g. GDB
- Efficient, Complete system environment for developing embedded software

What is in OVP?

- **Modeling APIs**
 - Publishing of C OVP APIs for Processor, Peripheral, and Platform modeling
 - Documentation & header files
- **Open Source library of models**
 - C source of models written to C OVP APIs
 - Processor models of ARM, ARC, MIPS, PowerPC, Renesas V850, M16c, Xilinx MicroBlaze, OpenRisc, SPARC, x86, ...
 - Peripheral models of standard embedded devices
 - Example embedded platforms in C, C++, SystemC, TLM2.0
 - Including full platforms that boot operating systems like uClinux, Linux, Nucleus, Micrium uC/OS-II, FreeRTOS
- **OVP reference simulator, free for non-commercial use**
 - Runs processor models fast, 500 MIPS typical
 - Interfaces to GDB via RSP/socket
 - MP Capable, scalable and very efficient
 - Can encapsulate existing processor models (ISS)
 - Callable with C/C++/SystemC/TLM2.0

OVP Summary



- The key to efficiency for future software development environments is the use of simulation and Virtual Platforms
- The availability of high performance, high quality models is critical
- The Open Virtual Platforms solution is increasingly important – especially with the move to MP
- The Imperas technology donation and formation of OVP kick starts a new phase in embedded software development
- OVP provides a fantastic OpenSource modeling solution to be the foundation of the next generation of software development environments
- Committed collection of partners developing the ecosystem
- ⇒ The most important opening & donation since SystemVerilog

Visit www.OVPworld.org

Timeline: 1977 (C), 1983 (C++), 1986 (GNU gcc / gdb), 1991 (Linux Open Verlog), 1999 (SystemC), 2001 (Open SystemVerlog), 2003 (Eclipse SystemVerlog), 2008.

Navigation: HOME, ABOUT, TECHNOLOGY, NEWS & EVENTS, DOWNLOAD, FORUMS, LIBRARY, COMPANIES, PLATFORMS, PROCESSORS, PERIPHERALS.

CategoryPeripheral :: PageIndex :: RecentChanges :: Change settings :: You are AdminStr

The following 20 pages belong to

- AddingNewComponents
- AllImperasPeripheralModels
- GenericRAM
- GenericROM
- GenericTRAP
- IntPIIX4E8259
- Library
- MaltaFPGA
- NicAM79C97x
- PciIDE
- PciPIIX4Ebase
- PciPM
- PciUSB
- Ps2Control
- RtcMC146818
- SmartDma
- SmartpromLinux
- SmartS412x

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Ask a Question

Moderators: None

Users browsing this forum: None

[new topic](#) [Open Virtual Platforms Forum Index -> Ask a Question](#)

Topics	Replies	Author	Views
some questions about your simulator	4	VahidLari	66
How to get a resistant team to engage?	2	markqaqolewski	51
OVPSim models estimating software performance	2	Zhonlei	38
Linux downloads	1	larryl	39
Building OS for OVP Platform	1	sibridge	28
Peripheral usage in Application	1	sibridge	23
Semi-hosting	1	BrianBailey	45
Can I simulate an OS with the simulator? Will it be slow?	2	riple	88
OVPSim vs. QEMU	1	jimc	84
Any differences with Proteus?	1	riple	63

Browser: Mozilla Firefox
URL: http://www.ovpworld2.org/index.php

Navigation: HOME, ABOUT, TECHNOLOGY, NEWS & EVENTS, DOWNLOAD, FORUMS, LIBRARY, RESOURCES, CONTACT.

LATEST (6th June 2008) - We have now announced a partnership with leading embedded processor IP vendor Tensilica - please see the associated press release and download/library pages of this web site.

We have also now put the source up of all the released Imperas peripheral models and OpenCores OR1K processor. Please click on the Library link above.

Recently several articles and industry comments have been added to the news section. There is a very good and comprehensive Technical Paper on Virtual Platforms by leading ESL consultant Brian Bailey - this is available to registered users on the main [download page](#) under Whitepapers list.

We are exhibiting OVP at DAC in Anaheim on the Imperas stand - if you are going - please drop in - then please come back to this site early next week for information about new forums that really make OVP usable.

We are just about to release a MIPS based platform that boots Linux 2.6 - this MIPS Linux



Timeline: 1977 (C), 1983 (C++), 1986 (GNU gcc / gdb), 1991 (Linux Open Verlog), 1999 (SystemC), 2001 (Open SystemVerlog), 2003 (Eclipse SystemVerlog), 2008.

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OVP Download MIPS

This page is dedicated to the MIPS processors. On the right you will see the different downloads available - simple single processor platforms running benchmark applications through to multi-core examples and also a Malta platform that boots Linux (not yet available).

Also - there is the download of the model itself - including many examples of using it - and its source.

Also there are GCC, GDB etc toolchains you will need to compile and run applications.

Using the OVP MIPS model

To use the MIPS model you will need several things downloaded. You will need to download a) the OVPSim simulator, b) the MIPS model itself, and c) if you don't already have the toolchain to compile up applications, you will need that too... And then take a look at some of the examples - they provide pointers as to what is needed for starter platforms. Then you will need to write your own platform.c file, application.c and when compiled - you will be all set.

MIPS Demo Slide Presentation [View Large](#)

You could walk through this presentation to get a feel for how easy it is to use the MIPS model. To find out more about the technology behind the model - please go to the Technology pages.



Open Virtual Platforms (OVP)

MIPS Demonstration Examples

MIPS Examples

Examples and demonstrations of different small applications/benchmarks running on platforms using MIPS processors

[Self contained MIPS demos \(1.3 MB\)](#)
Several simple example C programs running on MIPS processors. Includes single and multicore examples running fibonnaci, lnpack, dhrystone etc.

Multi-Core Platform Examples

Examples and demonstrations of different small applications/benchmarks running on different multicore platforms

[ARM7 and MIPS32 hetero multicore demo \(1.7 MB\)](#)
Simple platform with 1xARM7 and 3xMIPS32 processors with local and shared memory

MIPS Models

OVP Models of MIPS Processors, associated examples

[MIPS 32 Binary OVP model \(0.5 MB\)](#)
[MIPS 32 model normal and LE versions](#)

MIPS Toolchains

Compilers, linkers, debuggers for use with MIPS processors

[Compilers, linkers, debuggers for use with MIPS processors \(56 MB\)](#)
GNU GCC GDB etc for MIPS. Compiled versions of open source tools.

OVPSim Fast Free Simulator

Just-In-Time Code Morphing simulator that runs OVP models up to 500 MIPS for embedded software development.

[OVPSim \(7 MB\)](#)
Binary of the simulator, headers, examples of creating processors, peripherals and platforms, and running.

View the Presentations

INTRODUCTION

Introducing OVP
[www.OVPworld.org](#)
1 February 2008

ECOSYSTEM

What is being said about OVP?
[www.OVPworld.org](#)
February 2008

Latest Releases

[Imperas Announces Licensing, Distribution Relationship with Tensilica](#)
June 6th, 2008

[Open Virtual Platforms Heralds Start of New Era for Virtual Prototyping](#)
March 3rd, 2008

- Open Source models in Wikki based library, User Forums, Downloads, Presentations, [Documentation...](#)



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FREE MODELS,
EASY TO USE**

<http://www.ovpworld.org>

Enabling the next generation of
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